DG

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	((chip or IC or (integrated adj circuit)) with test$3) and (test adj signal$1 adj groups) and (combin$3 with test with signals) and (map$4 with (test adj signal$1)) and ((test adj signal$1) with output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 15:55
L2	2	((chip or IC or (integrated adj circuit)) with test$3) and (combin$3 with test with signals) and (map$4 with (test adj signal$1)) and ((test adj signal$1) with output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 15:55
L3	6	((chip or IC or (integrated adj circuit)) with test$3) and (combin$3 with signals) and (map$4 with (test adj signal$1)) and ((test adj signal$1) with output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 15:56
L4	6	((chip or IC or (integrated adj circuit)) with test$3) and (combin$3 with signals) and (map$4 with (test adj signal$1)) and ((test adj signal$1) with output) and multiplexer$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 16:00
L5	6	((chip or IC or (integrated adj circuit)) with test$3) and (combin$3 with signals) and (map$4 with (test adj signal$1)) and ((test adj signal$1) with output) and multiplexers	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 16:00
L6	3	((chip or IC or (integrated adj circuit)) with test$3) and (combin$3 with signals) and (map$4 with (test adj signals)) and ((test adj signals) with output) and multiplexers	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 16:07
L10	2	((chip or IC or (integrated adj circuit)) with test$3) and (map$4 with (test adj signals)) and (multiplexers with signals)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 16:44
L11	2	((chip or IC or (integrated adj circuit)) with test$3) and (test adj signal adj groups)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 16:44
L13	6	((chip or IC or (integrated adj circuit)) with test$3) and ((test adj signal) with groups) and multiplexers	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 17:25

L14	7	((chip or IC or (integrated adj circuit)) with test$3) and ((concurrent$2 or parallel or simultaneously) with (observ$3 or analyz$3 or verif$7) with (test adj signals))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 17:54
L20	26	((identical adj module$1) same (chip$1 or (integrated adj circuit$1) or IC)) and (test$3 same (IC or chip))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 18:15
L21	1	(byte adj lane adj mapping adj logic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 18:16
L22	1	(byte adj lane adj mapping) with logic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 18:16
L23	1	(byte adj lane adj mapping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 18:17
L24	1	(byte adj lane adj map$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 19:03
L25	3224	714/724.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 19:03
L26	851	714/736.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 19:04
L27	243	702/120.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 19:04
L28	1086	324/761.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/22 19:04